200G QSFP56 LR4 Transceiver Specification
HTQ56-31O8-10BD

Features

- Up to 26.5625Gbps data rate per channel by PAM4 modulation
- 4 duplex channels transmitters and receivers
- 4x26.5625 GBd PAM4 EML lasers
- Single +3.3V power supply
- SFF-8636 management interface
- Hot-pluggable QSFP56 form factor
- LC connector
- Low power dissipation:<8W
- QSFP+ 28 Gb/s compliant
- Operating temperature range: 0℃ ~ +70 ℃
- Compliant with ROHS

Applications

- 5G backhaul
- Switch & Router Connections
- Data Center 200GE 10km SMF links
- Other 200G Interconnect Requirements.

Standards

- IEEE 802.3bs
- CMIS V4.0
- QSFP56 MSA

Description

Hirundo’s 200G QSFP56 LR4 Transceiver is a high-performance solution for 200GE links for up to 10km over single mode fiber. It combines 4x 26.5625 GBd PAM4 electrical lanes into four 26.5625 GBd PAM4 optical channels in compliance with IEEE 200GBASE-LR4. Superior performance and reliability is achieved through advanced transmitter and receiver design using cooled EA-DFB-LDs each at a LWDM 1310nm wavelength and 4x PIN PDs with low-power TIAs. The 4 optical transmit and receive lanes are WDM’ed on to a single fiber pair through an LC connector.

1. Ordering Information

Table 1.1 Ordering Information

Part No.	Specifications									Application
	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Temp	Reach	Others	
HTQ56-31O8-10BD	QSFP56	200G	EML	-3.4 ~5.4dBm	PIN	<-7.7dBm	0~70 ℃	10km	RoHS	200G Base LR4
PN	HTQ56-31O8-10BD									
Description	200Gbps,SMF,10km,0-70℃									
SAP No	-									
Customer PN	-									

2. Revision History

Table 2.1 Revision History

Version	Initiated	Reviewed	Approved	Date
V1.0	Leo	Virgil	LiuSJ	2020.12.30

3. Absolute Maximum Ratings and Recommended Operating Conditions

Table 3.1 Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	5	95
Power Supply Voltage	Vcc	V	-0.5	+3.6

Table 3.1 Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	℃	0		70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Bit Rate(Per channel)	BR	GBd		26.5625	

4. Optical Specification

Table 4.1 Optical Specifications

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter (per Lane)						
Signaling Speed per Lane		GBd		26.5625		
Modulation format				PAM4		
Center wavelength		nm	1294.53		1310.19	LAN-WDM
Side-mode suppression Ratio	SMSR	dB	30			
Average Launch Power per Lane	TXPx	dBm	-3.4		5.3	
Total average launch power		dBm			11.3	
Tx OMA per lane	TxOMA	dBm	-0.4		5.1	
Launch power in OMAouter minus TDECQ(min)		dBm	-1.8			ER>=4.5dB
			-1.7			ER<4.5dB
$RIN_{21.4}$ OMA		dB/Hz			-136	
Optical Extinction Ratio	ER	dB	3.5			
Optical Return Loss Tolerance	ORL	dB			15.6	
Transmitter and dispersion eye closure (TDECQ),each lane	TDECQ	dB			3.2	
Average launch power of OFF Transmitter, each lane		dBm			-30	
Receiver(per Lane)						
Signaling Speed per Lane		GBd		26.5625		
Modulation format				PAM4		
Center wavelength		nm	1294.53		1310.19	LAN-WDM
Difference in receive power between any two lanes		dB			4.2	
Average receive Power per Lane	RXPx	dBm	-9.7		5.3	
Receive power, each lane (OMAouter)		dBm			5.1	
Receiver reflectance	Rfl	dB			-26	
Receiver sensitivity (OMA outer), each lane (max)		dBm			-7.7	
Stressed receiver sensitivity(OMAouter),each lane		dBm			-5.4	

5. Electrical Specification

Table 5.1 Electrical Specifications

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	VCC	V	3.135	3.3	3.465	
Supply Current	ICC	mA			2310	
Power Consumption		W			8.0	
Transmitter						
Data Rate	BR	GBd		26.5625		
Differential pk-pk input voltage tolerance		mV			900	
Differential termination mismatch					10%	
SCL and SDA High	VIH	V	2		3.5	
SCL and SDA Low	VIL	V	-0.3		0.8	
LPMode, ResetLand ModSelL High	VIH	V	2		3.5	
LPMode, ResetLand ModSelL Low	VIL	V	-0.3		0.8	
Receiver						
Data Rate	BR	GBd		26.5625		
Differential Output Swing	VRXDIFF	mV			900	
Differential termination mismatch					10%	
Near-end Eye height, differential	VEH	mV	70			
Near-end (Eye symmetry mask width)	ESMW	UI	0.2			
Transition time (20% to 80%)	T_r,T_f	ps	9.5			
INTL Output Voltage High	VOH	V	2		3.5	
INTL Output Voltage Low	VOL	V	0		0.8	
IIC communication						
IIC Clock frequency	-	KHZ	/	400	1000	
clock stretching	-	us	/	/	500	
Data hold time	-	ns	300	/	/	

6. Module Memory Map

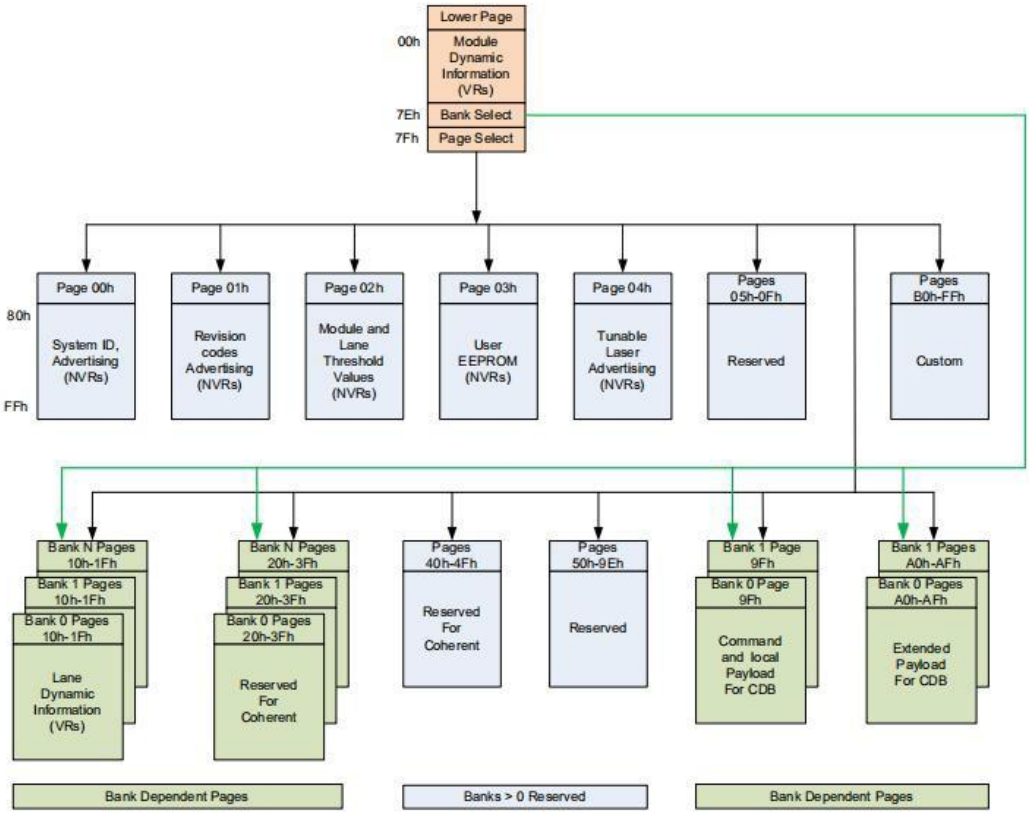


Figure 1 Digital Diagnostic Memory Map

7. Pin Assignment and Pin Description

7.1 Pin Assignment

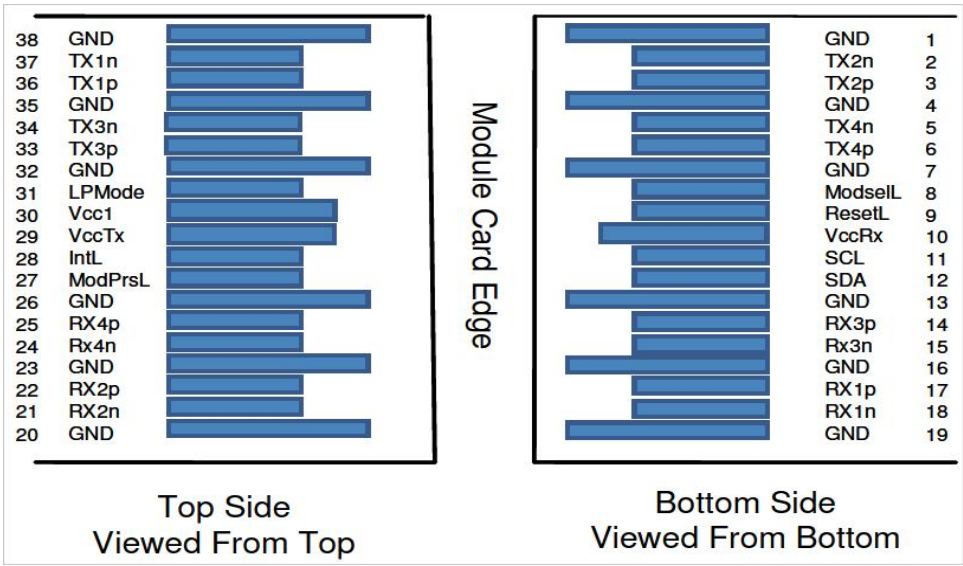


Figure 2. Electrical Pin-out Details

7.2 Pin Description

Pin	Symbol	Name/Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSe1L	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrSL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power Supply	

31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

1. QSFP56 uses common ground (GND) for all signals and supply (power). All the common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connected theses directly to the host board signal common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100pF.

8. Principle diagram

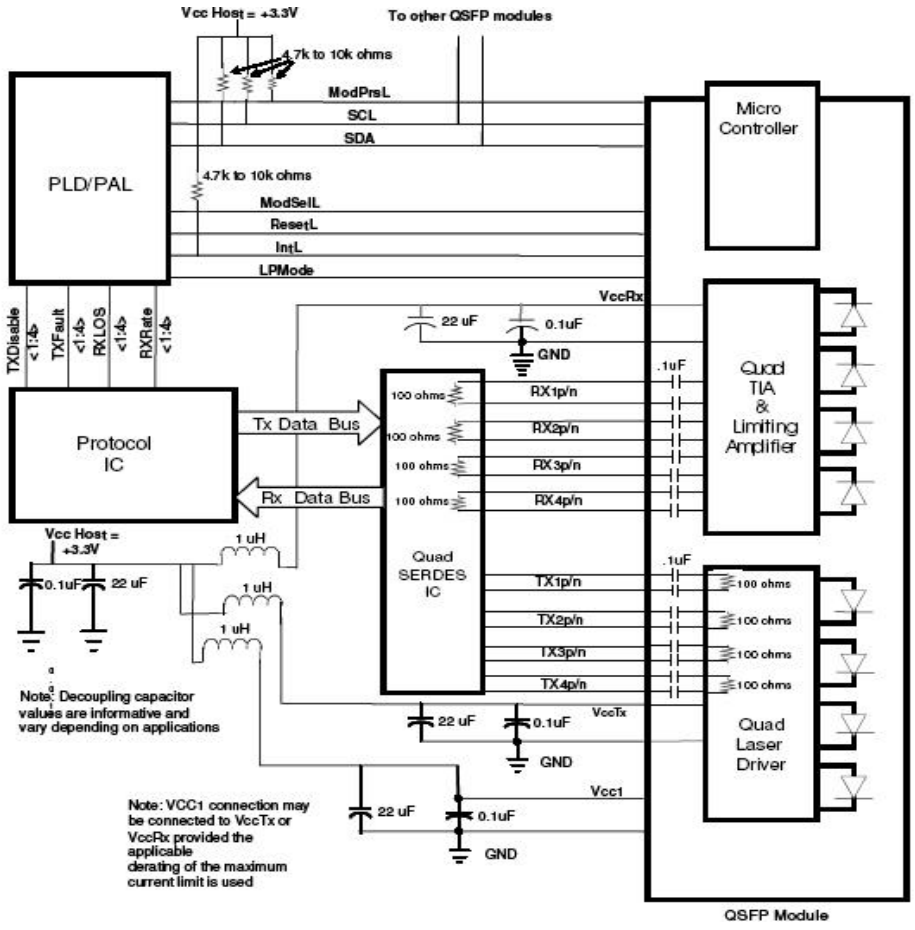


Figure 3. Module Principle Diagram

9. Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. Figure is the suggested transceiver/host interface.

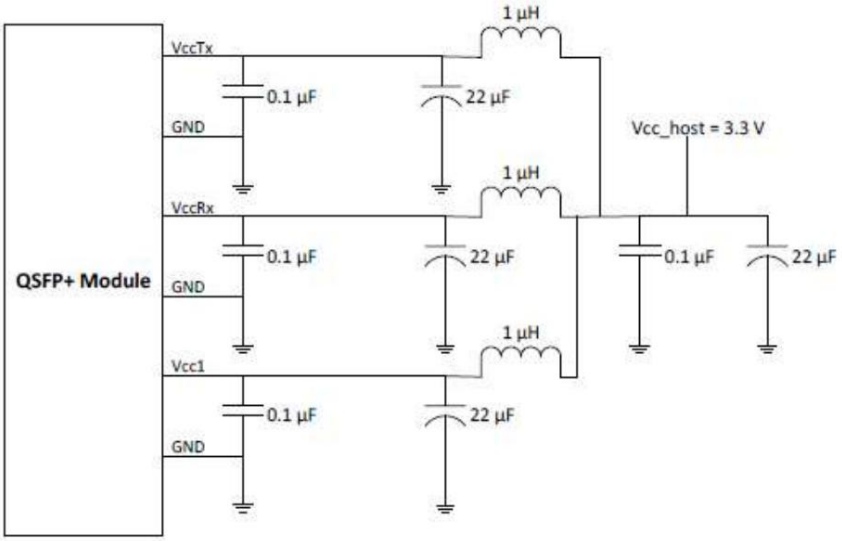


Figure 4 Recommended Host Board Power Supply Filtering

10. Package Outline

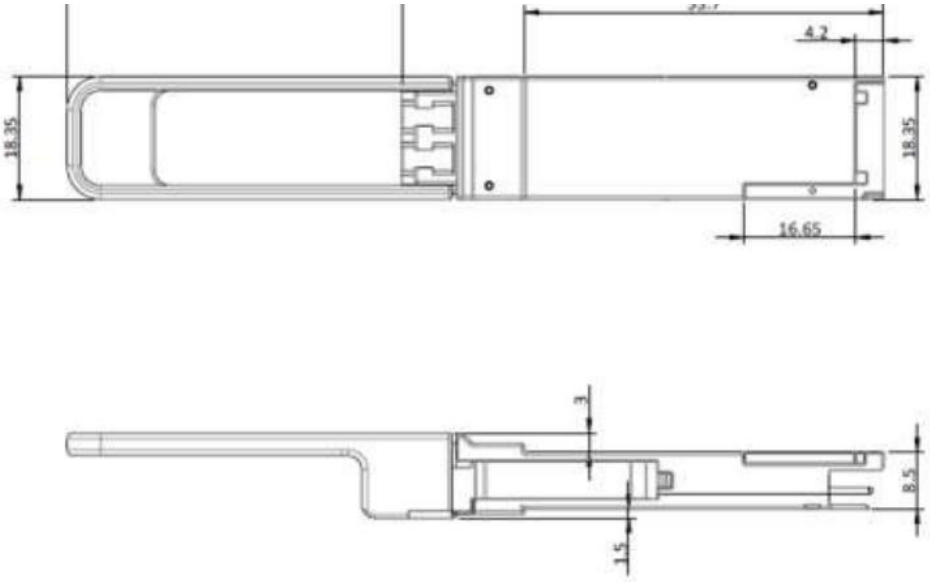
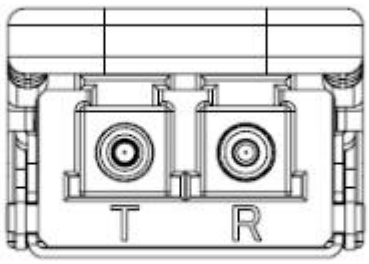


Figure 5 Package Outline

11. Package Outline



Looking into the connector, transmitter is on the left.

Figure 6. Optical lane sequence

12. For More Information

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